WATT-LEVEL MILLIMETER-WAVE MONOLITHIC DIODE-GRID FREQUENCY MULTIPLIERS

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ABSTRACT

Monolithic planar arrays containing in excess of 1000 Schottky diodes have produced watt level output at 66 GHz in a doubler configuration in excellent agreement with large signal predictions of the frequency multiplication. Current efforts are concentrated on fabricating and developing arrays of novel barrier-intrinsic-N^+ (BIN) diode which promise increased performance in tripler and quintupler configurations.

INTRODUCTION

Inexpensive watt level CW solid-state sources are required for a variety of millimeter and submillimeter wave applications. Available solid-state oscillators, such as GaAs Gunn diodes and IMPATTs, are highly efficient and tunable, but are currently limited to frequencies up to about 75 GHz and 150 GHz, respectively. Much higher frequencies can be obtained by generating harmonics of the fundamental frequency from solid-state oscillators operating at a lower frequency. This motivated our design of a diode grid for frequency multiplication (the theoretical diode multiplication efficiency is shown in Fig. 1). The approach [1] is attractive because a grid is monolithically integrated with thousands of Schottky diodes thereby resulting in potentially low-cost fabrication and small-size realization. In addition, it overcomes the power limitations of a single-diode multiplier because power is distributed among many diodes making possible watt level output power throughout the millimeter wave region.

SCHOTTKY DIODE DOUBLER ARRAY

Monolithic Schottky diode grids have been fabricated on 2-cm square GaAs wafers in a proof-of-principle test of a quasi-optical varactor millimeter wave frequency multiplier array concept [2] as illustrated in Fig. 2. An efficiency of 9.5% and output power of 0.5 W were achieved at 66 GHz when the diode grid was pumped with a pulsed source at 33 GHz [2]. Futhermore, the diode-grid equivalent circuit model based on a transmission-line analysis of plane wave illumination has been verified experimentally over a frequency range from 33 GHz to 140 GHz [3]. The equivalent circuit model together with a large-signal multiplier analysis [7] of the nonlinear varactor impedances were used to predict the doubler performance and to facilitate detailed comparison between theory and experiment.

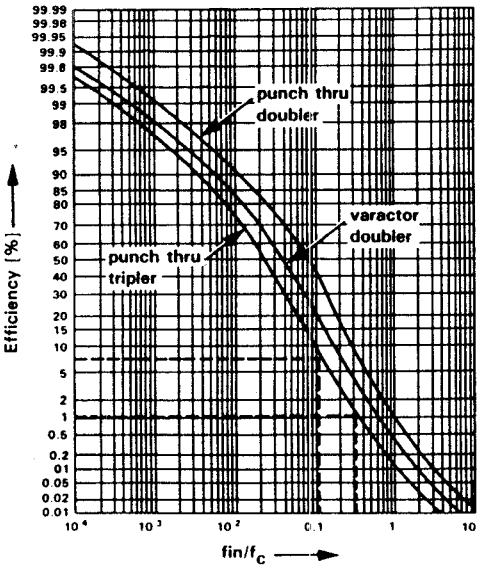

Fig. 1 Theoretical predictions of the doubler and tripler efficiencies of the punch through diode and the doubler efficiency of the varactor diode.

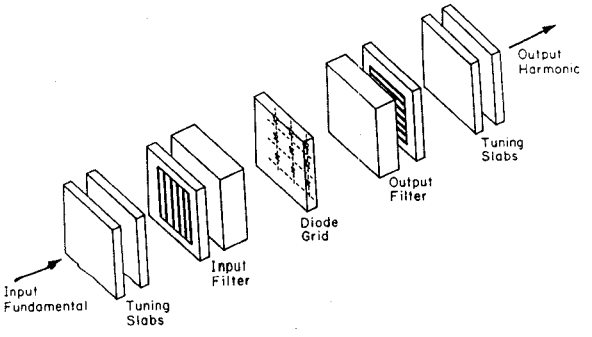

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Fig. 2 The quasi-optical varactor diode-grid doubler array design.

Excellent agreement was found between experiment and theory for a number of diode grids with ratio of pump to cutoff frequencies ranging from 0.1 to 0.32 as shown in Fig. 3. Here the triangles correspond to experimental measurements obtained using a simplified arrangement which consisted only of an input filter and tuning slabs at the output side of the array. Although simpler to implement than the configuration shown in Fig. 2, this structure does not permit a simultaneous optimum match at the pump and output frequencies. The diamonds correspond to corrections to the measurements accounting for the measured efficiency degradation associated with the simplified matching structure. The major limitations to the proof-of-principle diode grid arrays were the low diode breakdown voltage (≈ -3 V) and the high diode series resistance (= 25Ω - 50Ω). However, using currently realizable diode parameters we project CW doubling efficiencies of 60% at 66 GHz with output powers of 2 W using edge cooled wafers.

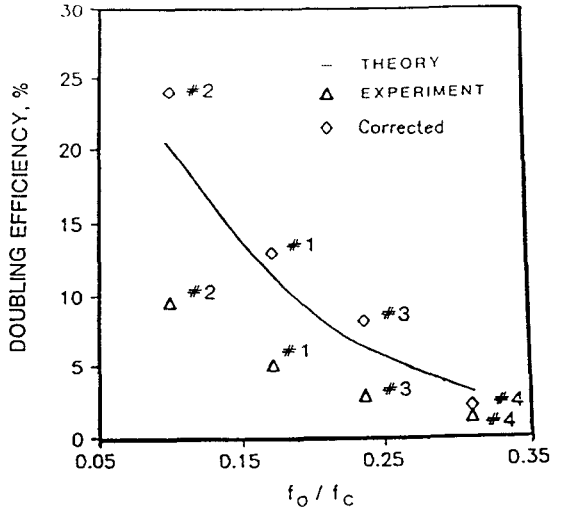

Fig. 3 A comparison of the measured Schottky diode doubling efficiencies with the Penfield and Rafuse theoretical predictions.

THIN MOS DOUBLER

In parallel with the GaAs Schottky diode doubler array studies, we investigated the use of a MOS structure having an undoped epitaxial layer, which is grown on a heavily doped substrate and isolated by a thin oxide layer [4]. The space-charge-limited current which is injected into the epilayer from the heavily doped substrate produces a step-like capacitance-voltage characteristic resulting in increased harmonic generation efficiency. The thin MOS concept was tested by fabricating honeycomb arrays which were mounted in crossed waveguide mounts and whisker contacted. Figure 4 shows the measured dependence in doubling efficiency (to 95 GHz) for a variety of dot radii as a function of pump power. The experimental results show good agreement with the theoretical predictions [5,6] and the large-signal multiplier analysis [7]. For example, a maximum efficiency of 17% was predicted for the 2 μm radius device which is in good agreement with the 14.7% obtained experimentally. Another important feature of these devices is that, due to the blocking barrier, two diodes can be operated back-to-back generating a sharp spike in the capacitance-voltage curve. The height and width of this capacitance-voltage characteristic can, in principle, be adjusted by doping control alone thus eliminating the need for an external dc bias. This arrangement needs no external ohmic contact resulting in a highly efficient frequency tripler. However, defects in the epitaxial silicon layer deteriorated the thin oxide and limited the yield of the devices making array construction difficult.

BIN DIODE TRIPLER ARRAY

Recently, a GaAs barrier-intrinsic-N^+ (BIN) diode has been developed [8] as shown in Fig. 5. This structure has an aluminum metal gate in intimate contact with a layered GaAs structure consisting of a 300 Å thickness of undoped GaAs, a 100 Å thick 10^{18} cm^{-3} heavily doped n^+ GaAs layer, another 1500 Å thickness of undoped GaAs, and a 3 μm 10^{18} cm^{-3} heavily doped n^+ GaAs region grown on top of a semi-insulating GaAs substrate. The GaAs BIN diode eliminates the problem of low fabrication yield associated with the thin MOS structure and takes advantage of the higher mobility of GaAs. It does not require an insulator layer as in the thin MOS structure but instead relies on a Mott-type barrier formed between the metal gate and a sheet of positive charge created by a thin (100 Å) heavily doped n^+ region in the GaAs. The 3 μm thick layer is required to reduce the series resistance. The active region is the intrinsic layer between the Mott barrier and the 3 μm heavily doped (10^{18} cm^{-3}) electron injection zone. A tripling efficiency of 35% at an output frequency of 100 GHz is predicted (as seen in Fig. 1) [5,6].

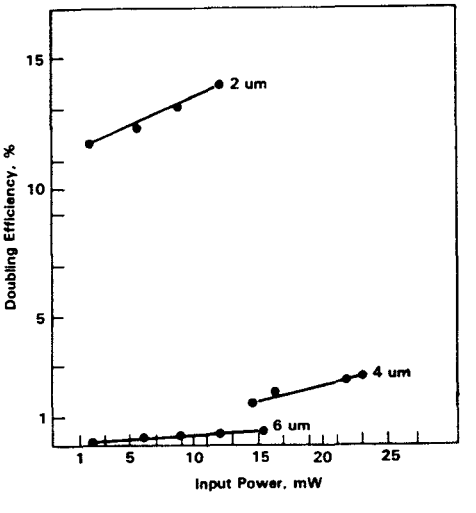

Fig. 4 Measured doubling efficiency (95 GHz output frequency) for various radii MOS devices.

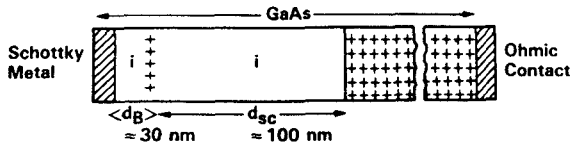

Fig. 5 The BIN diode structure.

The initial grid we designed for the BIN diode tripler consists of a square mesh of aluminum strips with Schottky electrodes on each end as shown in Fig. 6. The square mesh has a period of 500μm, each metal strip has a width of 20 μm, and each aluminum Schottky barrier varactor diode has an area of 10 μm^2. The small dimensions of the metal grid design can, therefore, provide the possibility of integrating more than 5000 diodes on a 2 inch wafer. The two neighboring Schottky electrodes are designed to give the back-to-back configuration for the BIN diodes. The grid requires only one metal pattern, which greatly facilitates the fabrication.

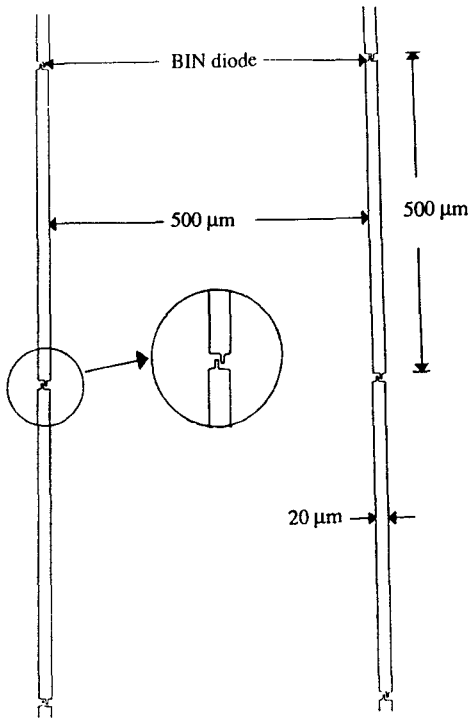

Fig. 6 The design of the metal grid for the BIN diode tripler array. The incident electrical field is assumed to be vertically polarized.

In support of the monolithic BIN diode array studies, a quasi-optical tripler design has been developed as shown in Fig. 7, where power at the fundamental frequency enters from the bottom left, through an input tuner and filter. The tilted dichroic plate (which functions as a high-pass transmission filter) reflects the incident pump power at the fundamental frequency to the diode grid on the left of it, and the metal mirror behind the diode again reflects all the harmonics back to the dichroic plate. The fundamental frequency and second harmonic are then blocked by the dichroic plate. In addition, the second harmonic is stopped by the input filter. The third harmonic, however, passes through the dichroic plate, through another tuning network, and leaves on the top right. For the laboratory tests, tuning slabs, filters and diode grids are all mounted on micrometers, so they can be easily positioned relative to each other. The tripler configuration has been tested with one of the remaining Schottky diode grids. However, since the diodes had relatively high series resistance ($\approx$ 107Ω), the efficiency was not predicted to be high. A third harmonic conversion efficiency of 0.5% was achieved at 99 GHz when the Schottky diode grid was pumped with a pulsed source at 33 GHz. This compares favorably with the predicted 1% from theory [5,6] and the large-signal multiplier analysis [7]. As a further note, it should be pointed out that this same Schottky array provided a 1.5% doubling efficiency in agreement with theory. Since this initial tripler configuration has not been optimized, we believe it will permit the extraction of the predicted output powers from the BIN diode grid array.

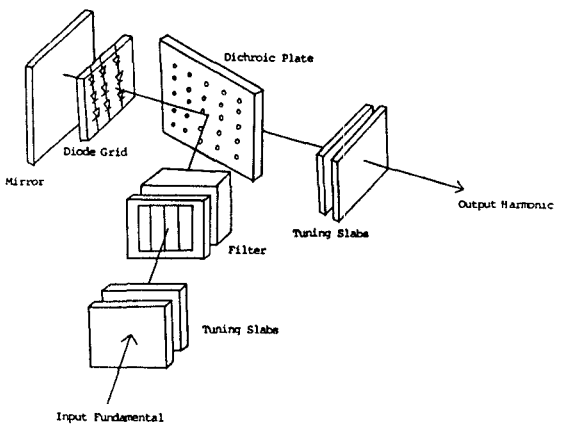

Fig. 7 The varactor diode grid tripler array design.

CONCLUSION

Based on the measurements of the quasi-optical frequency tripler array design, together with the studies of Schottky diode grid and thin MOS diode frequency doublers, we are confident in predictions of achievable watt level CW power from a new monolithic diode grid frequency tripler design employing the BIN diode concept.

ACKNOWLEDGEMENT

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